

NANOTUBE SEMICONDUCTOR DEVICES AND METHODS FOR MAKING THE SAME

Field of the Invention

5 The present invention relates to semiconductor devices including carbon nanotubes, such as a vertical nanotube transistor/capacitor cell.

Background of the Invention

10 There are continuing goals in semiconductor fabrication to reduce the number of masks or steps needed to fabricate semiconductor devices, e.g., memory cell devices such as DRAMs. Likewise, there is a continuing goal to shrink the size of such devices thereby maximizing the density of the resulting chip or die. Lastly, there is a desire to provide such devices that perform consistently.

15 There has been some recent interest in the use of carbon nanotubes due to their remarkable properties. Researchers have found carbon nanotubes to be stronger and tougher than steel, capable of carrying higher currents than either copper or superconductors, and able to form transistors a few nanometers across. In addition, nanotubes have high thermal conductivity and are stable at high temperatures. E. Lerner, Putting Nanotubes to Work, *The Industrial Physicist*, 22-25 (Dec. 1999). Further, carbon
20 nanotubes may have a consistent resistance (predicted to be about 6.0 kilohms) regardless of the length of the tube due to the intrinsic characteristics of ballistic transport in such nanotubes. A. Kasumov, Supercurrents Through Single-Walled Carbon Nanotubes, *Science*, 284, 1508-1510 (May 1999). Currently, the resistance of conventional semiconductor devices varies due to the doping means that are used to produce the desired resistance.
25 Thus, the consistent resistance of a nanotube would be of particular value for semiconductor devices. However, neither the form that particular nanotube semiconductor devices would take nor methods for mass production of nanotube semiconductor devices are currently known or available.

Summary of the Invention

The present invention provides vertical nanotube semiconductor devices and methods for making the same. An embodiment of the semiconductor devices of the present invention comprises a vertical transistor/capacitor cell including a nanotube (a hollow tube).

5 The device includes a vertical transistor and a capacitor cell both using a single nanotube to form the individual devices.

The present invention also provides a semiconductor device comprising vias for electrical interconnections between layers of integrated circuits. Specifically, an embodiment of a via according to the present invention may comprise a first trace layer, a
0 nanotube (e.g., a carbon tube) having a lower end connected to the first trace layer, the nanotube being substantially orthogonal to the first trace layer. A second trace layer is electrically connected to an upper end of the nanotube. Thus, the nanotube forms a via or electrical interconnection between the first and second trace layers.

The present invention also provides a semiconductor device comprising a
5 logic stack or multi-gate stack device including a stack of transistors formed about a vertical nanotube. The multi-gate stack may include two transistors in series, such as for an AND gate. The small size and predictable resistivity of the nanotubes used in this device provide unique advantages.

The present invention further provides methods for forming semiconductor
20 devices having multiple vertical nanotubes using patterned nucleation materials formed upon semiconductor substrates.

All of the specifically described methods and semiconductor devices are set forth for illustration of the methods and devices of the present invention. It is understood, however, that the present invention is not limited to those specifically described
25 embodiments of the methods and devices.

Brief Description of the Drawings

Fig. 1 is an embodiment of a vertical transistor/capacitor cell formed with a nanotube.

Figs. 2A-2I depict process steps for fabrication of an embodiment of a vertical transistor/capacitor cell array.

Fig. 3 is an embodiment of a nanotube via for a semiconductor device, e.g., a memory cell device.

5 Figs. 4A-4F depict the process steps for fabrication of an embodiment of a nanotube memory cell capacitor with a control transistor.

Fig. 5 is an embodiment of a nanotube logic stack for a semiconductor device, e.g., a memory cell device.

0 Detailed Description of the Invention

Certain embodiments of the invention are illustrated in the figures, like numerals being used to refer to like and corresponding parts of the devices and methods depicted in the various drawings.

The present invention provides semiconductor devices, such as vertical
5 transistor/capacitor cell devices, vias or interconnects, and vertical stacks of logic gates, wherein the devices include a nanotube, for example a carbon nanotube. Also provided are methods for fabrication of carbon nanotube semiconductor devices. The present invention need not be limited to the particular semiconductor devices illustrated in the figures nor the particular embodiments of the same. Other semiconductor devices or embodiments of the
10 semiconductor devices illustrated in the drawings may be formed using the methods of the present invention. For example, the devices and methods provided herein may include individual carbon nanotubes or collections of carbon nanotubes.

With the description as provided below, it is readily apparent to one skilled in the art that various processes described herein may be utilized in various configurations. For
15 example, the present invention may be used in the formation of transistors, capacitors, interconnections, etc. for semiconductor devices, particularly various memory devices. Exemplary vertical transistor/capacitor cells for DRAM structures and methods for making the same are described below. The same is true as to exemplary interconnects and logic stacks for use in semiconductor circuitry such as memory cells. It is to be understood that

these semiconductor structures and fabrication methods are only a few examples of many possible structures and methods for practice of the present invention. For example, carbon nanotubes are used to form the devices, but nanotubes formed of different materials may be used, such as silicon carbide. As another example, single or stacked capacitors could be
5 formed.

Further, although only DRAMS are mentioned specifically, this invention is applicable to other semiconductor devices and particularly to all areas of memory and memory access technology including logic devices and all RAM and ROM devices (e.g., DRAM, SRAM, SCRAM, EDRAM, VDRAM, NVSRAM, NVDRAM, DPSRAM,
0 PSDRAM).

An embodiment of a vertical transistor/capacitor cell 10 including a nanotube is shown in Fig. 1. The device shown may be used as a vertical transistor and a capacitor cell, both using a single nanotube 22, such as a carbon nanotube, to form the individual devices. More specifically, the vertical transistor/capacitor cell 10 shown in Fig. 1 includes
5 a substrate 12 having the desired circuitry (not shown) necessary to complete a memory cell array (such as an array as shown in Fig. 2I). A first insulation layer 14, comprising any suitable insulation material, e.g., silicon dioxide, covers the substrate 12 with a portion 38 of the substrate remaining exposed. A source 17 is connected at portion 38 to the external
circuitry (not shown) formed on the substrate 12. Likewise other portions of the
20 substrate 12 are left exposed for connection of a transistor gate 19 and drain 21 (discussed below) to the external circuitry of substrate 12.

The nanotube 22 is connected substantially orthogonal to an upper surface of the first insulation layer 14. The vertical transistor portion of structure 10 depicted in Fig. 1 includes a source 17 and an annular gate 19 insulated from nanotube 22. Gate 19 is
25 connected to external circuitry (not shown) on the substrate 12. The transistor further includes a channel formed by the nanotube 22, and an annular drain 21 connected to the nanotube 22 and to external circuitry (not shown) on the substrate 12. An isolation layer 20, comprising boron nitride or any other suitable insulating material, covers exposed portions of an exterior wall of nanotube 22. As is known to those skilled in the art, isolation layer 20

may comprise plural layers. The plural layers of insulation 20 may be deposited at different steps in the construction of a device such as the transistor/capacitor cell 10 so as to separate or insulate the source 17, gate 19, drain 21 from one another and from portions of the substrate 12.

5 As known to those persons skilled in the art, various components of the vertical transistor/capacitor cell structure 10 shown in Fig. 1 may be of a variety of dimensions depending upon the device properties desired. For example, an embodiment of structure 10 may have the following dimensions: the nanotube 22 (preferably a carbon nanotube) may have an internal diameter of from about 0.6 to greater than about 5
0 nanometers and a length of from about 1 to about 2 microns. The insulation layer 14 may be from about 0.1 to about 1 micron in thickness. The source 17, gate 19, and drain 21 may be from about 0.25 to about 1 micron in thickness, and insulator 20 may range from about 0.002 to about 0.5 micron in thickness.

 In particular embodiments, the device 10 depicted in Fig. 1 may be used as a
5 transistor. As with typical transistors, the gate 19 controls current flowing through the nanotube 22 (i.e., the channel) between the source 17 and drain 21.

 Similarly, in particular embodiments, the device 10 depicted in Fig. 1 may be used as a capacitor. The source 17 allows the nanotube 22 to receive a potential. Thus, the source 17 may serve to charge the capacitor while nanotube 22 serves as a capacitor cell
20 storing the charge. Charge may be directed to and drained away from the cell (nanotube 22) by control of gate 19. The nanotube 22 acting as the cell allows the capacitor to store charge on interior walls of the nanotube as well as on the exterior walls, thereby increasing storage capacity as compared to the typical semiconductor capacitor.

 Thus, each nanotube 22 forms both a channel of a vertical transistor and a
25 cell for the capacitor. That is, due to the unique properties of nanotubes, a single nanotube may serve as a dielectric material and form a capacitor cell, and serve as a semiconductor material and form a transistor channel in the same device. Not only does the nanotube device provide superior physical characteristics (e.g., consistent resistance) the nanotubes also allow formation of much smaller semiconductor devices, thereby reducing the overall

size of computer dies. Further, due to the consistency in resistance of the nanotubes, unlike conventional devices, the devices of the present invention will be consistent device-to-device, die-to-die, and wafer-to-wafer.

A method for making an array of the vertical transistor/capacitor cell structures 10 shown in Fig. 1 is depicted in Figs. 2A-2I. All depositions, etches, reflows, etc. are performed by conventional methods (unless otherwise stated) as known to those persons skilled in the art. Likewise, as is understood by those skilled in the art, materials forming components of the described structures are not limited to those explicitly cited but may comprise any suitable material for the function performed by the component.

With reference to Fig. 2A, a substrate 12 is provided. Substrate 12 is formed from any suitable material that may serve to form substrates for semiconductor devices. Useful substrate materials include, but are not limited to, doped or undoped silicon, doped or undoped polycrystalline silicon, gallium arsenide, gallium phosphide, and indium phosphide. The substrate 12 is then treated to form desired circuitry for the final device, to which the vertical transistor/capacitor cell structures 10 (as shown in Fig. 1) will be connected, such as a memory device decoding network.

With reference to Fig. 2A, a first insulation layer 14 is formed over the substrate 12. The first insulation layer 14 may comprise any insulating material capable of functioning as an insulator or a dielectric in a semiconductor device. Exemplary insulating materials to form the first insulation layer 14 include, but are not limited to silicon dioxide, tetraethyl orthosilicate (TEOS), nitrides, and oxides. Alternatively, plural insulating materials may be employed to form insulation layer 14.

A nucleation layer 16 is then applied to cover the first insulation layer 14. The nucleation layer 16 may be formed by a single application or by plural applications of suitable nucleation materials. Nucleation layer 16 may comprise any material capable of nucleating growth of a nanotube. For example, nickel, cobalt and iron are known catalysts for the growth of carbon nanotubes. A particularly useful composition for the nucleation of carbon nanotube growth comprises $\text{Fe}(\text{NO}_3)_3 \cdot 9\text{H}_2\text{O}$, $\text{MoO}_2(\text{acac})_2$ and alumina nanoparticles.

A patterning layer 18 is then formed over the nucleation layer 16 and is patterned, developed, and etched such that the areas of the nucleation layer 16 upon which nanotubes 32 are to be formed are exposed (Fig. 2B). The patterning layer 18 may comprise any suitable masking material, such as polymethylmethacrylate (PMMA). The procedure of Kong et al., Synthesis of Individual Single-walled Carbon Nanotubes on Patterned Silicon Wafers, *Nature*, **395**, 878-881 (Oct. 1998), incorporated herein by reference, may be employed to grow the nanotubes. Kong et al., pattern PMMA on silicon and deposit nanotube growth nucleating material as a solution. After vaporization of residual solvent, the PMMA is removed and the resulting "catalytic islands" are subjected to chemical vapor deposition (CVD) conditions for nanotube growth.

The nanotubes 22, preferably but not necessarily carbon nanotubes, may be formed, e.g., by plasma state methods or (CVD). For example, in CVD atoms of the nucleation layer 16 that are exposed to the vapor act to form the nanotubes by attaching themselves to a growing edge of the tube beneath a catalyst cap 28 (Fig. 2C). The nanotubes 22 will grow substantially vertically, i.e., substantially orthogonal to the substrate 12 (Fig. 2C). Further, the nanotubes 22 will grow only where the nucleation layer 16 is exposed. The nanotubes 22 form hollow tubes having a wall thickness of from about 0.6 nm to about 3 nm and an internal diameter of from about 0.6 nm to about > 5 nm. As the nanotubes 22 are formed the exposed portions of the nucleation layer 16 move up with the top portion or upper ends of the nanotubes, forming caps 28 thereon. Patterning layer 18 may then be removed (Fig. 2D).

With reference to Fig. 2E, the caps 28 formed by the portions of the nucleation layer 16 exposed during the nanotube 22 growth may then be removed by etching or other suitable means. The nanotubes 22 are connected to the external circuitry on the substrate 12 by forming conductive rings 40, such as metal rings, about the nanotubes 22 (Fig. 2F). The conductive rings 40 are in direct physical contact with a portion of an outer surface of the nanotubes 22. Undesirable conductive material deposited on the nanotubes 22 during formation of the conductive rings 40 may be removed in any suitable manner as known to those persons skilled in the art. The conductive rings 40 provide necessary

electrical connection of the nanotubes 22 to the circuitry (not shown) previously formed on the substrate 12.

With reference to Fig. 2G, a second insulation layer 44 is formed over the nanotube 22 and conductive rings 40. The second insulation layer 44 is formed to protect the nanotube 22 from oxygen in oxidizing environments. The second insulation layer 44 may comprise any insulative material that can be applied below 2800° C in a vacuum or less than 750° C in air.

With reference to Fig. 2H, another conducting material is deposited to form a second set of conductive rings 46 about each insulated nanotube 22. Second conductive rings 46 form annular gates (gate 19 in Fig. 1) and comprise any suitable conductive material. The second conductive rings 46 do not directly contact the nanotube 22, but are insulated therefrom by insulation layer 44. With reference to Fig 2H, a third insulating layer 47 is formed over the second conductive rings 46.

Finally, a follow-on patterning is performed to create the vertical transistor. Specifically, with reference to Fig. 2I, the insulating layer 44 is patterned to expose a portion of nanotube 22 such that a third layer of conductive material may be deposited to form a third set of conductive rings 48. The third conductive rings 48 have direct physical contact with the nanotube 22. The third conductive rings 48 form the drains (drain 21 in Fig. 1) for the vertical nanotube transistors. A third insulation layer 49 is then deposited to protect the vertical transistor from oxygen and other contaminants.

Another embodiment of the nanotube semiconductor device of the present invention comprises vertical vias for electrical interconnections between layers of integrated circuits. Specifically, with reference to Fig. 3, an embodiment of a via 50 according to the present invention may comprise a first plane or substrate 52, whereupon desired circuitry (not shown) has been formed. A first trace layer 54 covers a portion of substrate 52. A nanotube 22 (e.g., a carbon nanotube) is connected to the first trace layer 54 and is substantially orthogonal to the first plane 52. A second trace layer 60 covers an upper portion of the nanotube 22 and extends therefrom. The nanotube 22 thus forms a via 50 or electrical interconnection between the first and second trace layers 54 and 60. With

reference to Fig. 3, the material 56 between the trace layers 54, 60 may comprise any suitable insulation material described above in relation to other embodiments or known to those skilled in the art. Material 56 essentially comprises the layers of an integrated circuit through which the vias are being formed. In addition to the embodiment shown in Fig. 3,
5 the nanotube vias may be arrayed parallel to the substrate to provide an electrical interconnection of the desired consistent resistance.

The via devices of the present invention provide the same advantages over conventional semiconductor devices as those discussed above in relation to the vertical transistor/capacitor cell device. Specifically, the nanotube vias provide connections having
0 consistent resistance values and may be much smaller than conventional vias or interconnection devices. The individual vias of the present invention offer predictable resistance, governed by quantum mechanics, of about 6 kohm independent of length. Similarly, arrays of nanotube vias provide a means of predictably varying the resistance between a given pair of trace layers.

15 With reference to Fig. 4F, an embodiment of the present semiconductor device may comprise a memory cell capacitor device 37. The device 37 preferably comprises a substrate 12 having therein the desired circuitry (not shown), an insulation layer 14, and a nanotube 22, e.g., a carbon nanotube. In this particular embodiment the nanotube comprises a carbon nanotube having a hemispherical carbon cap 33. Nanotube 22
20 is connected to source 17, and thereby electrically connected to the external circuitry of the substrate 12 at exposed portion 38 (having external circuitry). An annular gate 19 is electrically connected to the substrate 12 at connection 39. A ground cell plate 35 is provided and is electrically connected to the substrate 12 at connection 26 (an opening through insulation layer 14). Isolation material 20 insulates the source 17, gate 19 and
25 ground cell plate 35.

With reference to Fig. 4F, the source 17 allows the nanotube 22 to receive a potential. The nanotube 22 forms a capacitor cell and may be used as a dielectric. The annular gate 19 controls the effective cross section of the nanotube capacitor cell 22. The effective cross section may be reduced to zero by applying the appropriate potential at

annular gate 19. A charge may thus be formed and maintained on the memory cell capacitor device 37 across the nanotube 22 between the source 17 and ground cell plate 35.

With reference to Figs. 4A-4F, a memory cell capacitor device 37 with a control transistor including a source 17 and gate 19 may be constructed using, e.g., the following process steps. A substrate 12 having the desired circuitry (not shown) and an insulation layer 14 are provided. A nanotube 22 is provided by, e.g., the method set forth above in relation to the transistor/capacitor cell device array as shown in Fig. 2I. Following the formation of the nanotubes 22, a catalyst cap 32 remains at a growing edge of the nanotube 22 (Fig. 4A). The catalyst cap 32 may, optionally, be removed and the nanotube 22 left open. Alternatively, the nanotube 22 may be resubjected to suitable nanotube growth conditions, such as those described above with reference to Fig. 2C, to form the hemispherical carbon cap 33 on the nanotube as shown in Fig. 4B.

The insulation layer 14 is patterned as known to those skilled in the art to expose a portion 38 of the substrate 12. The source 17 is formed between the nanotube 22 and the substrate 12 at exposed at 38 as depicted in Fig. 4B (such that the source 17 is connected to external circuitry exposed on the substrate. With reference to Fig. 4C, an isolation layer 20 comprising, for example boron nitride or other suitable insulating material is formed.

A portion 39 of the substrate 12 may then be exposed by a patterning procedure as known to those skilled in the art, and an annular gate 19 formed to encircle nanotube 22 (Fig. 4D). An additional isolation layer 20 is then deposited (Fig. 4E) to insulate the annular gate 19. The additional isolation layer 20 may be deposited over a sublayer of isolation material. The additional isolation layer 20 may comprise any suitable insulating material described in relation to other embodiments above or known to those skilled in the art. The insulation layer 14 is patterned as known to those skilled in the art to expose ground cell plate connection 26 on substrate 12, and ground cell plate 35 comprising aluminum, copper or other conductive material is formed (Fig. 4F).

Another embodiment of the nanotube semiconductor device of the present invention comprises a logic stack 70 (or multi-gate stack), such as used in an AND gate, as

shown in Fig. 5. Such a logic stack 70 may include a substrate 72 comprising any suitable material (as discussed above) that may serve to form substrates for semiconductor devices and a first insulating layer 14 comprising any suitable material (as discussed above). The substrate 72 is treated to form desired circuitry (not shown), to which the final device, the
5 logic stack structure 70 (as shown in Fig. 5) will be connected.

With reference to Fig. 5, the logic stack device 70 comprises two transistors in series formed using a single nanotube 22. Source 77 and two annular gates 79 and 81 are formed about a common nanotube 22. A drain 83 connects the nanotube to the substrate 12. The source 77 may be formed as described above for the memory cell capacitor (Fig. 4B).
0 As shown in Fig. 5, the nanotube 22 is ringed by the two separate insulated gates 79 and 81. Connection of the drain 83 and insulating layer 20 completes the logic stack 70.

The logic stack device 70 may function in similar fashion as a conventional AND gate. The gates control the flow of current through the nanotube 22 (acting as the channel for the transistors) between source 77 and drain 83.

15 Whereas the invention has been described with reference to multiple embodiments and representative methods, it will be understood that the invention is not limited to those specific embodiments and methods. On the contrary, the invention is intended to encompass all modifications, alternatives, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.